# Notice of References Cited Application/Control No. | Applicant(s)/Patent Under | Reexamination | ACAR ET AL. | Examiner | Art Unit | Page 1 of 2

# **U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-6,687,883	02-2004	Cohn et al.	716/4
	В	US-6,711,719	03-2004	Cohn et al.	716/2
	С	US-2004/0230924	11-2004	Williams et al.	716/002
	D	US-2003/0177460	09-2003	Chen	716/5
	E	US-6,427,226	07-2002	Mallick et al.	716/10
	F	US-			
	G	US-			,
	Н	US-		·	
	ı	US-			
	J	US-			
	к	US-			
	L	US-			
	М	US-			

## **FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	10.				
	0					
	Р					
	Q					
	R					
	S	,				
	Т					

### **NON-PATENT DOCUMENTS**

		No. 1
*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Mill-Jer Wang et al., "Guardband determination for the detection of off-state and junction leakages in DRAM testing", 19-21 Nov. 2001, Test Symposium, Proceedings. 10th Asian, Digital Object Identifier 10.1109/ATS.2001.990274, Page(s):151 - 156
	v	Liu et al., "Power supply current detectability of SRAM defects", 23-24 Nov. 1995, Test Symposium, Proceedings of the Fourth Asian, Digital Object Identifier 10.1109/ATS.1995.485362,□□Page(s):367 - 373 □□
	w	De Salvo et al., "Experimental and theoretical investigation of nonvolatile memory data-retention", July 1999, Electron Devices, IEEE Transactions on, Volume 46, Issue 7, Digital Object Identifier 10.1109/16.772505, Page(s):1518 - 1524
	×	Thibeault et al., "A novel probabilistic approach for IC diagnosis based on differential quiescent current signatures", 27 April-1 May 1997, VLSI Test Symposium, 15th IEEE, Digital Object Identifier 10.1109/VTEST.1997.599445, Page(s):80 - 85

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

# Notice of References Cited Application/Control No. | Applicant(s)/Patent Under | Reexamination | ACAR ET AL. | Examiner | Art Unit | Page 2 of 2

## **U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-			
	В	US-			
	С	US-		·	
	D	US-			
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	К	US-			
	L	US-			
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# FOREIGN PATENT DOCUMENTS

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0				·	
	P		,			
	Ω					
	R					·
	S				·	
	.Т					

# **NON-PATENT DOCUMENTS**

		NON-FATENT DOCUMENTS
*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Mukhopadhyay et al., "Modeling and estimation of total leakage current in nano-scaled CMOS devices considering the effect of parameter variation", 2003, ISBN:1-58113-682-X, ACM Special Interest Group on Design Automation, Pages: 172 - 175
	٧	Sirichotiyakul et al., "Duet: An Accurate Leakage Estimation and Optimization Tool for Dual-Vt Circuits", APRIL 2002, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 10, NO. 2, Pages: 79 -90
	w	Lee et al., "Simultaneous State, Vt and Tox Assignment for Total Standby Power Minimization", 2004, IEEE/ACM Design, Automation and Test Europe, Pages: 494-499□□
	х	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.